

Universal Magnetic-Core Logic Elements



FEATURES

- **HIGHEST "LOGIC POWER"** — Unequalled per-element functional flexibility; each element provides up to six discrete input modes without supplemental circuitry of any kind.
- **MAXIMUM NOISE IMMUNITY** — Inherently low impedance level of element circuitry ensures high 1 : 0 ratios and a minimum of pulse distortion. Circuitry inherently reshapes pulse at every interrogation.
- **MINIMUM POWER-SUPPLY REQUIREMENTS** — Lowest ratio of average power to peak output power of any available digital element. Only one, unregulated, unipolar voltage required for all circuits... no clamps, taps, bias returns, or decoupling networks required.
- **NON-VOLATILE STORAGE** — Logical state of the circuitry is retained during power failure of any kind.
- **SMALL . . . LIGHT . . . TOUGH** — Highest functional-density of any macroelement. Optimum shape and proportions for high-density card mounting.

Encapsulated for complete environmental protection, maximum shock and vibration resistance, and low internal thermal gradient.

- **HIGHEST OBTAINABLE CIRCUIT RELIABILITY** — Digital magnetic circuitry, which has been developed by DI/AN to a high degree of sophistication, is inherently extremely reliable. DI/AN magnetic elements have fewer components and fewer solder joints, and are completely encapsulated. In addition, over its many years of experience, DI/AN has developed production and testing techniques which ensure optimum product performance and reproducibility from lot to lot. A concentrated quality assurance program includes life testing, component evaluation and 100% production testing. Quality control standards conform to requirements of MIL-Q-9858. RESULT: more than 8 million module hours of operation without a failure.

- **PROVEN IN THOUSANDS OF APPLICATIONS** — Write for booklet entitled "Magnetic Logic in Space (A Report of Applications and Reliability)".

GENERAL DESCRIPTION

DI/AN CTL's are *universal* logic elements with integral magnetic storage and delay capability. Appropriately interconnected, without additional circuitry of any kind, they can perform any logical function. A single DI/AN CTL (Core Transistor Logic element) will implement any of the following logic functions: AND, OR, INHIBIT (AND NOT), BRANCH, TRANSFER, DRIVE, BINARY COUNT and COMPLEMENT. Only two CTL's are required to implement the EXCLUSIVE-OR function — and four CTL's form a full adder.

Because the CTL utilizes only a small number of components (and those few being non-critical components with wide operating margins), it provides a reliability unmatched by any other logic element. The ability of this single, basic element to handle all logic functions provides the ultimate in logic

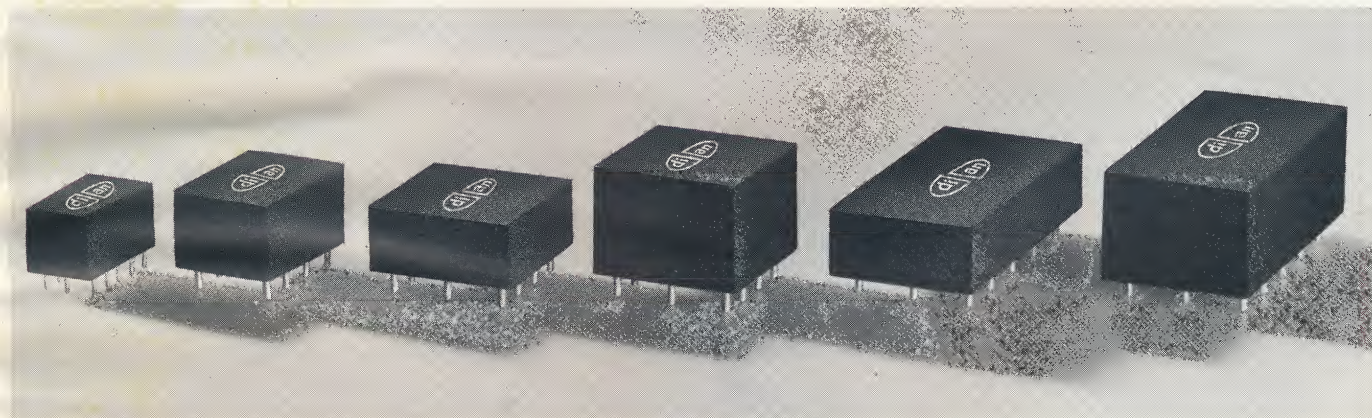
design simplicity, minimizing inventory problems and lowering costs at several stages of the design and production process.

The CTL offers the designer many other important advantages. Aging is negligible. Power supply requirements are minimal. Circuit packaging is convenient and inexpensive. Operating margins are wide, yet unit-to-unit performance control is very tight, which makes for easier, more straightforward designs that can be pushed to the limit. The CTL, in fact, is a very forgiving device, with broad tolerance for the poor waveforms, noise, etc., that plague the marginal circuit.

PRINCIPLES OF OPERATION

DI/AN Magnetic Core Logic Elements are simple in design and construction. They consist of a magnetic core containing

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CHARACTERISTICS — MAGNETIC CO

Model Designation	Packaging	Operating Freq. Range kilobits/sec	Maximum Operating Temp. (°C)	Power Supply Requirements (Nominal)			Inputs (Nominal)				
				Voltage $\pm 15\%$	Power (mW) All "ONE's"	Power (μ W) Stand By	Information			Voltage	
							Current			E_{in} (volts)	Z_{in} (Ω)
							I_{in} (ma)	Voltage Drop Across Winding	Duration (μ sec)		

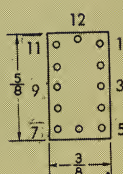
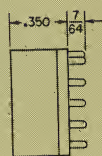
LOGIC ELEMENTS

CTL-100-P/N-12 CTL-100-P-3I-12 CTL-100-N-3I-12	SQ	0-100	55	12	140	60	20	1.2	5	—	—
CTL-100-P/N-12S**	SQ	0-100	75	12	150	75	15	0.8	4	—	—
CTL-250-P/N-12 CTL-250-P-3I-12 CTL-250-N-3I-12	SQ	0-250	55	12	250	60	30	1.0	2	—	—
CTL-100-P/N-24 CTL-100-P-3I-24 CTL-100-N-3I-24	LSQ	0-100	125	24	280	30	18	1.5	5	—	—
CTL-100-P/N-24	PB	0-100	125	24 $\pm 25\%$ —10%	150	25	12	0.5	4	—	—
CTL-250-P/N-24	LSQ	0-250	125	24	400	30	30	0.8	2	—	—
CTL-250-P-3I-28	PB	0-250	100	28	300	30	25	0.8	2	—	—
CTL-250-P/N-28	PB	0-250	100	28	300	30	25	0.8	2	—	—
CTL-250-P-4I-2S-28	MPB	0-250	100	28	300	30	25	0.8	2	—	—

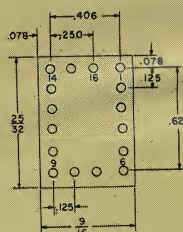
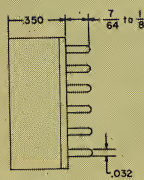
ACCESSORY ELEMENTS

CTI-100-P-12	DSQ	0-100	55	12	400	60	—	—	—	—1.5 to —15	2000
CTI-250-P-12	DSQ	0-250	55	12	500	100	—	—	—	—1.5 to —15	3000
CTI-100-P/N-24	LDSQ	0-100	100	24	625	185	—	—	—	+2.5	3000
CTI-250-P/N-24	LDSQ	0-250	100	24	750	200	—	—	—	+2.0	3000
CTP-5-P-12	DSQ	0-5	55	12	840	84	—	—	—	—1.5 to —10	250
CTP-5-P-24	DSQ	0-5	100	24	1500	125	—	—	—	—5 to —20	250
TDL-100-24	LSQ	0-100	100	24	—	—	—	—	—	—	—

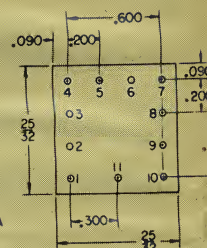
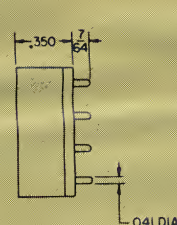
PICO-BIT®
(PB)



MODIFIED PICO-BIT®
(MPB)



LOW SQUARE
(LSQ)



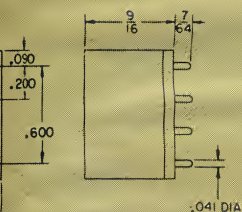
CORE LOGIC ELEMENTS & ACCESSORIES*

Trigger				Outputs (Nominal)							Logic Capability		
				Voltage			Current				Fan Out		
				Amplitude (volts)	1:0 Ratio	Permissible Z load (Ω/pf)	Undelayed		Delayed		Trigger Using Delay Network	Trigger Not Using Delay Network	Information from Delay Network
Duration (μ sec)	I_{in} (ma)	IZ Drop Across Wdg. (volts)	Duration (μ sec)				I peak (ma)	Duration (μ sec)	I peak (ma)	Duration (μ sec)			
—	100	0.25	0.5	12	15:1	2000	100	0.5	30	4	—	—	—
—	100	0.25	1.0	11	20:1	2000	100	1.0	20	4	—	—	—
—	100	3.0	0.25	11.5	25:1	1500	100	0.25	30	0.85	—	—	—
—	100	0.8	0.5	23	20:1	3000	100	0.5	30	3.0	—	—	—
—	100	0.8	0.5	21	25:1	4000	100	0.5	30	1.5@20ma	—	—	—
—	100	1.0	0.3	23	30:1	3000	100	0.3	30	1.4	—	—	—
—	100	1.0	0.8	22	30:1	3000	150	0.5	30	1.4	—	—	—
—	100	1.0	0.8	22	30:1	3000	150	0.5	30	2.0	—	—	—
—	100	1.0	0.8	22	30:1	3000	150	0.5	30	2.0	—	—	—
2.0††	—	—	—	-2.5	—	100	100	1.5	30	4	4	10	4
1.0	—	—	—	-4	—	200	130	0.5	30	1.0	4	15	4
0.5	—	—	—	+6	—	400	160	0.7	30	3.5	4	20	4
0.5	—	—	—	+6	—	400	125	0.45	30	1.5	4	20	4
1.0	50 to 200	0.2	1.0	—	—	—	200	30 min	—	—	10 (A)	6 (B)	20 (C)
1.0	50 to 200	0.4	1.0	—	—	—	250	17 min	—	—	10 (A)	6 (B)	20 (C)
—	from CTL			—	—	—	100	0.5	—	—	—	20	—

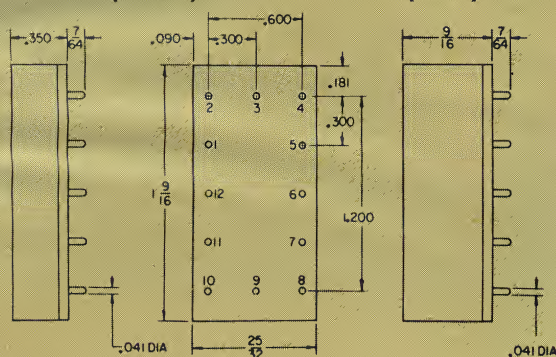
**Available on special order: high reliability device qualified to APOLLO Specs; $T \leq 105^{\circ}\text{C}$

††Beyond Threshold — (A) Via Input — (B) Reset via D.N. — (C) Via Shift

SQUARE (SQ)



LOW DOUBLE-SQUARE (LDSQ) DOUBLE SQUARE (DSQ)



Model Designation Code (use in ordering)

Output Polarity
P/N = Either Positive-Going or Negative-Going Output Pulse.
P = Positive-Going Output Pulse
N = Negative-Going Output Pulse
Nominal Power-Supply Voltage
Module Package

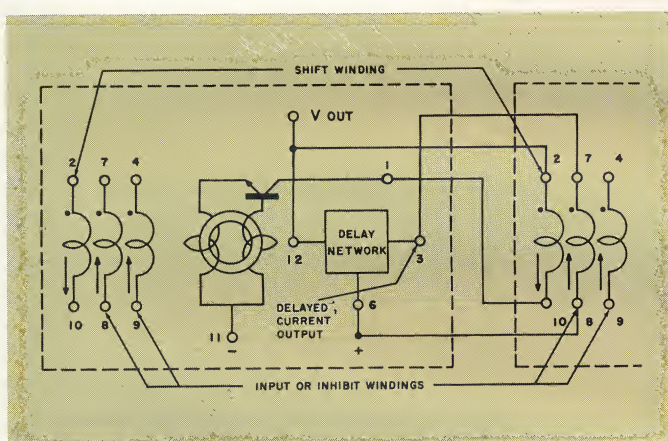
CTL-100-()-()-12()-()

Maximum Repetition Rate (Kilobits/Sec)
Number of Logical Inputs (if more than two). Use only when Output Polarity specified is either "P" or "N"
Write an "S" here when specifying Silicon

*For additional information, please write for pertinent Module Specification Drawing.

several windings, a transistor operated as a switch, and a simple passive delay network. Each CTL contains two or more information inputs, one or more shift inputs, and three types of outputs: (1) an undelayed voltage, which can be used to set static flip-flops, drive one-shots, etc.; (2) an undelayed current, ordinarily used to shift other CTL's; and, (3) a delayed current, commonly used to load or inhibit other CTL's.

Toroidal ferrite cores, having a rectangular hysteresis loop are employed in all DI/AN Magnetic Logic Elements. These cores have the ability to store information in the form of a stable residual magnetic field. An appropriate input pulse (applied to an *input winding*) will create a field that sets the core to the ONE condition. The application of a shift pulse to another winding (the *shift winding*) will, if of the correct polarity, reverse the magnetic field, resetting the core to ZERO. This flux reversal generates an output signal in the other windings on the core. Subsequent shift pulses of the established output polarity produce no significant output until the core is again set to the ONE state.



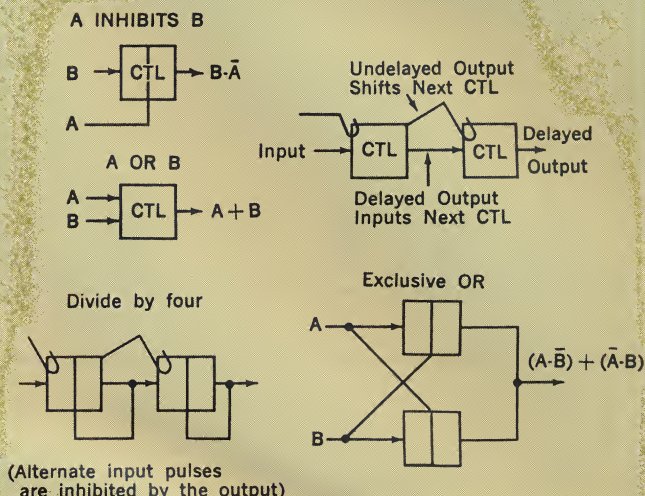
CTL shown wired for negative output to shift and load following CTL. Single CTL is enclosed by dotted line. Positive output achieved by simple change in external wiring. Pin numbers correspond to base diagram for the Pico-Bit®. Arrows show input direction.

The CTL module provides a connection arrangement that allows the transistor output to be directed through the shift windings of subsequent CTL's prior to being applied to its own delay network. This assures that the shift output precedes the load or inhibit output, thus preventing interaction between the shift and load (or inhibit) pulses. Connections are available on each CTL to provide either a positive or a negative output for a stored ONE.

SPECIAL ELEMENTS AND ACCESSORIES

CTI input amplifiers combine the functions of power amplification and signal-amplitude discrimination. Their input characteristics resemble a Schmitt trigger circuit. They are commonly used either to shift-and-load CTL's by amplifying low-energy signals that could not perform this function directly. A delay network is provided in the CTI for use in the shift-and-load operation. The CTI provides con-

ELEMENTARY APPLICATIONS (Write for Applications Handbook)



stant-amplitude, constant-width, output pulses essentially independent of input-signal waveshape or repetition rate.

CTP elements operate as "pulse stretchers" and "pulse fortifiers", and are used to preset or reset one or more magnetic core circuits, through either their input or shift windings. The CTP input can be either a voltage or a current pulse (not to occur simultaneously nor at a rate in excess of 5 KC) — the output is a current pulse of relatively long duration.

TDL pulse amplifiers are used to generate CTL shift pulses, when driven by the undelayed current output of another CTL. The use of this accessory circuit is recommended when it is logically necessary to shift more CTL's than can be driven by the unamplified, undelayed-current output pulse from one CTL.

CTRO elements are wide-pulse, high-peak-power pulse generators designed to furnish the current required to drive relay coils. Compatible with the CTL, they also have the logic capability of shift register elements. In a common application, CTRO's are connected in a shift register configuration in which a single ONE is stored. From this circuit, a predetermined sequence of relay closures can be obtained, as determined by the system logic. The output pulse width produced by a CTRO is controlled by an external timing capacitor, which can serve several CTRO's on a time-sharing basis.

These accessory modules are available in electrical and environmental ratings compatible with any of the standard DI/AN Magnetic-Core Logic Elements. Please feel free to consult the DI/AN Applications Engineering Department for specific circuit advice.



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